Dielectric characteristics

Class I Dielectrics

Multilayer Ceramic Capacitors are generally divided into classes which are defined by the capacitance temperature characteristics over specified temperature ranges. These are designated by alpha numeric codes. Code definitions are summarised below and are also available in the relevant national and international specifications.

Capacitors within this class have a dielectric constant range from 10 to 100. They are used in applications which require ultra stable dielectric characteristics with negligible dependence of capacitance and dissipation factor with time, voltage and frequency. They exhibit the following characteristics:-

a) Time does not significantly affect capacitance and dissipation factor (Tan δ) – no ageing.
b) Capacitance and dissipation factor are not affected by voltage.
c) Linear temperature coefficient.

		Class I Dielectrics						
		C0G/NP0 (Porcelain)	P90 (Porcelain)	C0G/NP0		X8G	Class I High Temperature	
Dielectric classifications		Ultra stable	Ultra stable	Ultra stable		Ultra stable	Ultra stable	
	IECQ-CECC	-	-	1B/CG		-	-	-
	EIA	C0G/NP0	P90	C0G/NP0		X8G	-	-
	MIL	-	-	CG (BP)		-	-	-
Ordering code	DLI	CF	AH	-	-	-	-	-
	Novacap	-	-	-	N, RN	-	F	D, RD
	Syfer	-	-	Q, U	C	H	-	G
	Voltronics	F	H	Q	-	-	-	-
Rated temperature range		-55ºC to +125ºC	-55ºC to +125ºC	-55ºC to +125ºC	-55ºC to +125ºC	-55ºC to +150ºC	-55ºC to +160ºC	-55ºC to +200ºC
Maximum capacitance change over temperature range	No DC voltage applied	0 ±15 ppm/ºC	0 ±20 ppm/ºC	0 ±30 ppm/ºC	0 ±30 ppm/ºC	0 ±30 ppm/ºC	0 ±30 ppm/ºC	0 ±30 ppm/ºC
	Rated DC voltage applied	-						
Tangent of loss angle (tan δ)		≤0.0005 @1MHz		≤0.0005 @1MHz	>50pF ≤0.0015 ≤50pF $0.0015\ (\frac{15}{Cr} + 0.7)$	≤0.0005 @1MHz	≤0.001	
Insulation resistance (Ri)	Time constant (Ri x Cr)	@25ºC = 10^6 MΩ min @125ºC = 10^5 MΩ min		100GΩ or 1000s (whichever is the least)			@25ºC = 100GΩ or 1000ΩF @160ºC & 200ºC = 1GΩ or 10ΩF (whichever is the least)	
Capacitance Tolerance	Cr <4.7pF	±0.05pF, ±0.10pF, ±0.25pF, ±0.5pF						
	Cr ≥4.7 to <10pF	±0.10pF, ±0.25pF, ±0.5pF						
	Cr ≥10pF	±1%, ±2%, ±5%, ±10%						
Dielectric strength Voltage applied for 5 seconds. Charging current limited to 50mA maximum.	≤200V	2.5 times	2.5 times	2.5 times				
	>200V to <500V			Rated voltage +250V				
	500V to ≤1kV			1.5 times				
	>1kV to ≤1.2kV		N/A	1.25 times				
	>1.2kV			1.2 times				
Climatic category (IEC)	Chip	-	-	55/125/56		-	-	
	Dipped	-	-	-	55/125/21	-	-	
	Discoidal	-	-	-	55/125/56	-	-	
Ageing characteristic (Typical)		Zero						
Approvals	Syfer Chip	-	-	-	QC-32100	-	-	

Dielectric characteristics

Class II Dielectrics

Capacitors of this type have a dielectric constant range of 1000-4000 and also have a non-linear temperature characteristic which exhibits a dielectric constant variation of less than ±15% (2R1) from its room temperature value, over the specified temperature range. Generally used for by-passing (decoupling), coupling, filtering, frequency discrimination, DC blocking and voltage transient suppression with greater volumetric efficiency than Class I units, whilst maintaining stability within defined limits.

Capacitance and dissipation factor are affected by:-

a) Time (Ageing)
b) Voltage (AC or DC)
c) Frequency

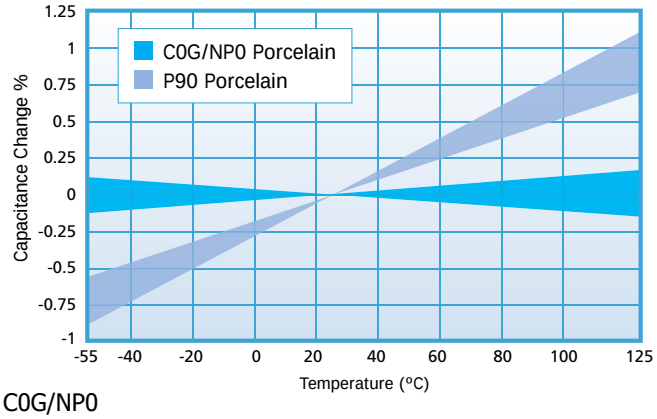
Class II Dielectrics								
X5R	X7R			X8R	Class II High Temperature			
Stable	Stable			Stable	Stable			Dielectric classifications
-	2C1	2R1	2X1	-	-	-	IECQ-CECC	
X5R	-	X7R	-	X8R	-	-	EIA	
-	BZ	-	BX	-	-	-	MIL	
-	-	-	-	-	-	-	DLI	Ordering code
BW	-	B, RB	X	S	G	E, RE	Novacap	
P	R	X	B	N	-	X	Syfer	
-	-	X	-	-	-	-	Voltronics	
-55ºC to +85ºC	-55ºC to +125ºC			-55ºC to +150ºC	-55ºC to +160ºC	-55ºC to +200ºC		Rated temperature range
±15%	±15%	±15%	±15%	±15%	+15 -40%	+15 -65%	No DC voltage applied	Maximum capacitance change over temperature range
-	+15 -45%	-	+15 -25%	-	-	-	Rated DC voltage applied	
≤ 0.025 Typical*	>25V ≤0.025 ≤25V ≤0.035			≤0.025	≤0.025			Tangent of loss angle (tan δ)
100GΩ or 1000s (whichever is the least)							Time constant (Ri x Cr)	Insulation resistance (Ri)
±5%, ±10%, ±20%								Capacitance Tolerance
2.5 times							≤200V	Dielectric strength Voltage applied for 5 seconds. Charging current limited to 50mA maximum.
Rated voltage +250V							>200V to <500V	
1.5 times							500V to <1kV	
1.2 times							≥1kV	
55/85/56	55/125/56			55/150/56	-		Chip	Climatic category (IEC)
-	55/125/21			-	-		Dipped	
-	55/125/56			-	-		Discoidal	
5% Typical	<2% per time decade							Ageing characteristic (Typical)
-	QC-32100	-	-	-	QC-32100	-	Syfer Chip	Approvals

* Refer to page 61 for details of Dissipation Factor.

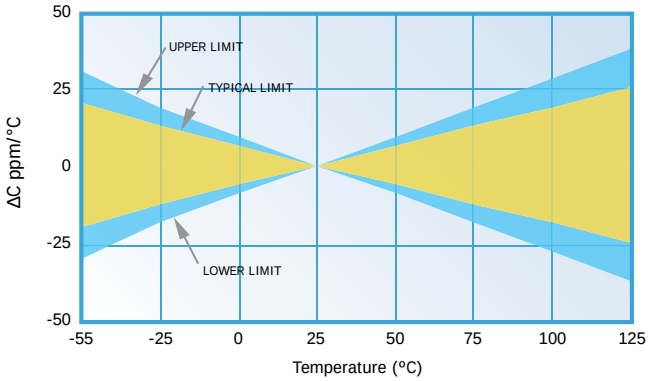
Dielectric characteristics

Typical dielectric temperature characteristics

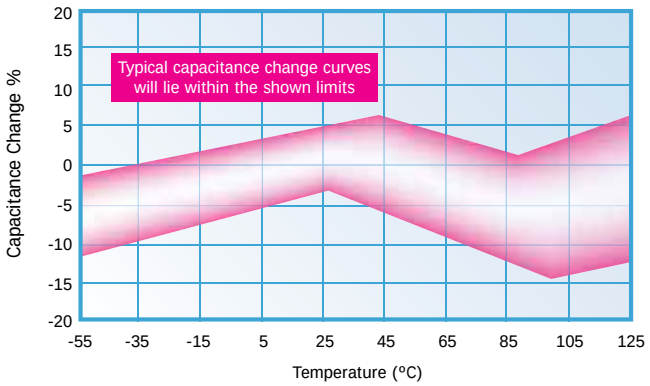
Porcelain C0G/NP0 & P90



C0G/NP0

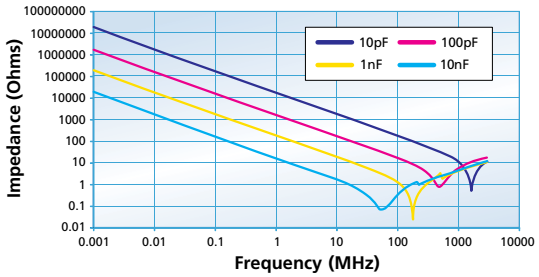


X7R

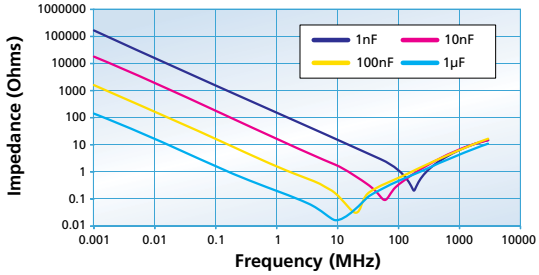


Impedance vs Frequency

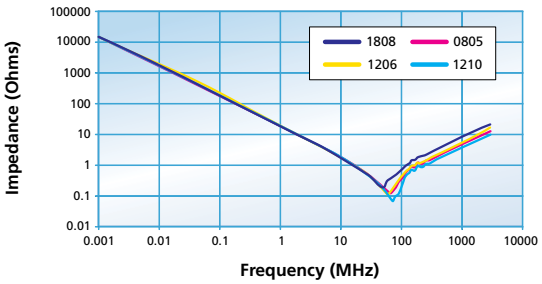
Ultra Stable C0G/NP0 dielectric



Stable X7R dielectric

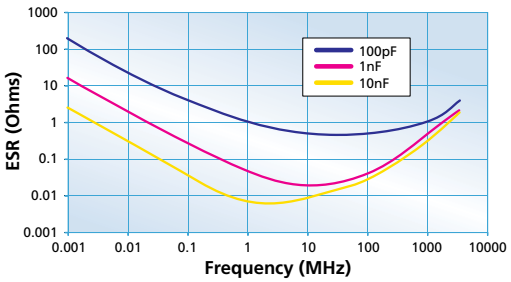


Stable X7R dielectric - 10nF

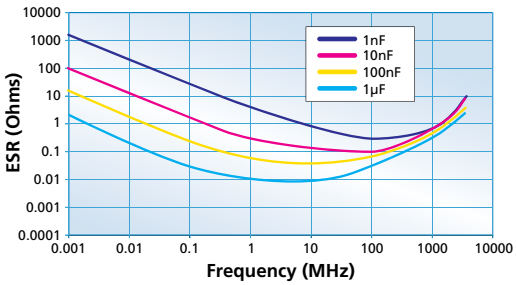


ESR vs Frequency - chips

Ultra Stable C0G/NP0 dielectric



Stable X7R dielectric



Dielectric characteristics - Porcelain C0G/NP0 & P90

Typical ESR and Series Resonance characteristics

CF Porcelain (C0G/NP0) and AH Porcelain (P90)

Dielectric	DLI Series	Cap (pF)	Typical ESR			Series Resonance (MHz)
			150 MHz	500 MHz	1 GHz	
CF TCC (ppm/°C) (-55° to +125°C) Porcelain (C0G/NP0) 0 ±15	C06CF 0603	1	0.182	0.276	0.428	10300
		10	0.095	0.159	0.243	3200
		47	0.081	0.127	0.173	1400
	C11CF 0505	1	0.073	0.089	0.146	9900
		10	0.049	0.075	0.107	3100
		100	0.040	0.073	0.111	970
	C17CF 1111	1	0.073	0.082	0.124	9060
		10	0.065	0.098	0.136	3100
		100	0.041	0.070	0.102	1300
		1000	0.034	0.073	–	400
	C18CF 1111	1	0.068	0.086	0.158	9060
		10	0.058	0.087	0.118	3100
		1000	0.041	0.068	–	1000
	C22CF 2225	10	0.072	0.113	0.164	2480
		100	0.047	0.079	0.119	1000
		1000	0.036	0.067	–	320
		2700	0.035	–	–	214
			10MHz	30MHz	100MHz	
	C40CF 3838	10	0.121	0.054	0.037	2100
		100	0.044	0.038	0.045	680
		1000	0.032	0.036	0.038	210
		5100	0.011	0.016	0.040	95

Dielectric	DLI Series	Cap (pF)	Typical ESR			Series Resonance (MHz)
			150 MHz	500 MHz	1 GHz	
AH TCC (ppm/°C) (-55° to +125°C) Porcelain (P90) +90 ±20	C11AH 0505	1	0.067	0.08	0.136	9200
		10	0.044	0.071	0.104	3000
		100	0.032	0.055	0.086	1000
	C17AH 1111	1	0.059	0.063	0.114	9064
		10	0.039	0.06	0.085	3100
		1000	0.024	0.05	0.074	1290
	C18AH 1111	10	0.059	0.094	0.138	3100
		100	0.028	0.069	0.109	1290
		1000	0.023	0.063	–	400
	C22AH 2225	10	0.074	0.207	0.249	2480
		100	0.048	0.116	0.19	1000
		1000	0.028	0.14	–	320
		2700	0.027	–	–	214
			10MHz	30MHz	100MHz	
	C40AH 3838	15	0.066	0.033	0.027	2100
		100	0.018	0.026	0.052	680
		1000	0.009	0.017	0.033	210
		5100	0.008	0.016	0.033	95

Dielectric termination combinations

		Palladium Silver	Palladium Silver	Nickel Barrier (100% matte tin plating). Lead free	Nickel Barrier 90/10% tin/lead	Nickel Barrier Gold flash	FlexiCap™ with Nickel Barrier 100% tin	FlexiCap™ with Nickel Barrier 90/10% tin/lead	FlexiCap™ with Copper Barrier 100% tin	FlexiCap™ Ag Layer, 400-u-in Cu barrier 200-u-in Sn Plate	FlexiCap™ with Copper Barrier 90/10% tin/lead	Copper Barrier 100% tin	Ag Layer, 400-500u-in Cu barrier, 200-u-in 90/10 Sn Plate	Copper Barrier 90/10% tin/lead	Solderable Silver	Solderable Palladium Silver	Ag termination, Ni Barrier, Heavy SnPb Plated Solder	Ag termination, Enhanced Ni Barrier, Sn Plated Solder	Ag termination, Enhanced Cu Barrier, Sn Plated Solder	Ag Termination, Cu Barrier Layer, Heavy SnPb Plated Solder
			RoHS	RoHS		RoHS	RoHS		RoHS			RoHS			RoHS	RoHS		RoHS	RoHS	
Recommended for Solder Attachment				●	●		●	●	●	●	●	●	●	●	●	●	●	●	●	●
Recommended for Conductive Epoxy Attachment		●	●			●														
Termination ordering code:	**DLI**	-	P	Z	U	S	Q	Y	M	-	-	W	-	V	-	-	T	E	H	R
	Novacap	P	PR	N	Y	NG	C	D	-	-	-	B	-	E	S	K	-	-	-	-
	Syfer	-	F	J	A	-	Y	H	3	-	5	2	-	4	-	-	-	-	-	-
	Voltronics	-	S	-	-	-	-	-	3	M	-	2	W	-	-	-	-	-	-	-
Dielectric	**Code**																			
NP0 Porcelain - Hi Q	DLI - CF		●	●	●	●	●	●				●		●			●	●	●	●
P90 Porcelain - Hi Q	DLI - AH		●	●	●	●	●	●	●			●		●			●	●	●	●
C0G - Hi Q/Low ESR	Syfer - Q, U			●	●															
C0G - Hi Q/Low ESR BME	Syfer - H			●																
C0G/NP0	Novacap - N/RN	●	●	●	●	●	●	●							●	●				
	Syfer - A			●	●		●	●												
	Syfer - C, F		●	●	●		●	●												
C0G/NP0 - BME	Syfer - G, K			●	●		●	●												
C0G/NP0 - Non-Mag	Novacap - M	●	●									●		●		●				
	Syfer - C, Q								●		●	●		●						
	Voltronics - Q		●							●		●	●							
X5R	Syfer - P		●	●	●		●	●												
	Novacap - BW			●	●	●														
X7R	Novacap - B/RB	●	●	●	●	●	●	●							●	●				
	Syfer - E						●	●												
	Syfer - X, D		●	●	●		●	●												
X7R - BME	Novacap - BB			●	●	●														
	Syfer - J			●			●	●												
	Syfer - S						●	●												
BX	Novacap - X	●	●	●	●	●	●	●							●	●				
	Syfer - B		●	●	●		●	●												
BZ	Syfer - R		●	●	●		●	●												
X7R - Non-Mag	Novacap - C	●	●									●		●		●				
	Syfer - X								●		●									
	Voltronics - X		●						●	●			●							
X8R	Novacap - S	●	●	●	●		●	●							●	●				
	Syfer - N		●	●	●		●	●												
	Syfer - T						●	●												
C0G/NP0 (160°C)	Novacap - F	●	●	●	●		●	●							●	●				
C0G/NP0 (200°C)	Novacap - D														●	●				
C0G/NP0 (200°C)	Novacap - RD			●																
	Syfer - G			●																
Class II (160°C)	Novacap - G	●	●	●	●		●	●							●	●				
Class II (200°C)	Novacap - E														●	●				
	Novacap - RE			●																
	Syfer - X			●																

Dielectric codes in **Red** - AEC-Q200 qualified. Dielectric codes in **Green** - IECQ-CECC.

FlexiCap™ overview

FlexiCap™ termination

MLCCs are widely used in electronic circuit design for a multitude of applications. Their small package size, technical performance and suitability for automated assembly makes them the component of choice for the specifier.

However, despite the technical benefits, ceramic components are brittle and need careful handling on the production floor. In some circumstances they may be prone to mechanical stress damage if not used in an appropriate manner. Board flexing, depanelisation, mounting through hole components, poor storage and automatic testing may all result in cracking.

Careful process control is important at all stages of circuit board assembly and transportation - from component placement to test and packaging. Any significant board flexing may result in stress fractures in ceramic devices that may not always be evident during the board assembly process. Sometimes it may be the end customer who finds out - when equipment fails!

Knowles has the solution - FlexiCap™

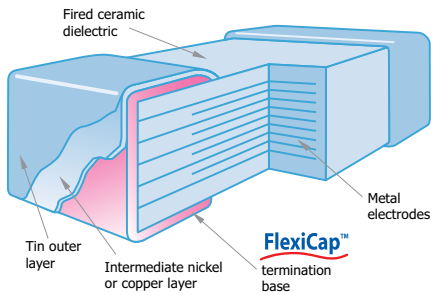
FlexiCap™ has been developed as a result of listening to customers' experiences of stress damage to MLCCs from many manufacturers, often caused by variations in production processes.

Our answer is a proprietary flexible epoxy polymer termination material, that is applied to the device under the usual nickel barrier finish. FlexiCap™ will accommodate a greater degree of board bending than conventional capacitors.

Knowles FlexiCap™ termination

Ranges are available with FlexiCap™ termination material offering increased reliability and superior mechanical performance (board flex and temperature cycling) when compared with standard termination materials. Refer to Knowles application note reference AN0001. FlexiCap™ capacitors enable the board to be bent almost twice as much before mechanical cracking occurs. Refer to application note AN0002.

FlexiCap™ is also suitable for Space applications having passed thermal vacuum outgassing tests. Refer to Syfer application note reference AN0026.



FlexiCap™ MLCC cross section

FlexiCap™ benefits

With traditional termination materials and assembly, the chain of materials from bare PCB to soldered termination, provides no flexibility. In circumstances where excessive stress is applied - the weakest link fails. This means the ceramic itself, which may fail short circuit.

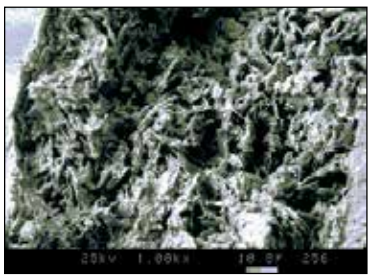
The benefit to the user is to facilitate a wider process window - giving a greater safety margin and substantially reducing the typical root causes of mechanical stress cracking.

FlexiCap™ may be soldered using your traditional wave or reflow solder techniques including lead free and needs no adjustment to equipment or current processes.

Knowles has delivered millions of FlexiCap™ components and during that time has collected substantial test and reliability data, working in partnership with customers world wide, to eliminate mechanical cracking.

An additional benefit of FlexiCap™ is that MLCCs can withstand temperature cycling -55ºC to 125ºC in excess of 1,000 times without cracking.

FlexiCap™ termination has no adverse effect on any electrical parameters, nor affects the operation of the MLCC in any way.



- Picture taken at 1,000x magnification using a SEM to demonstrate the fibrous nature of the FlexiCap™ termination that absorbs increased levels of mechanical stress.

Available on the following ranges:

- All High Reliability ranges
- Standard and High Voltage Capacitors
- Open Mode and Tandem Capacitors
- Safety Certified Capacitors
- Non-magnetic Capacitors
- 3 terminal EMI chips
- X2Y Integrated Passive Components
- X8R High Temperature capacitors

Summary of PCB bend test results

The bend tests conducted on X7R have proven that the FlexiCap™ termination withstands a greater level of mechanical stress before mechanical cracking occurs.

The AEC-Q200 test for X7R requires a bend level of 2mm minimum and a cap change of less than 10%.

Product X7R	Typical bend performance under AEC-Q200 test conditions
Standard termination	2mm to 3mm
FlexiCap™	Typically 8mm to 10mm

Application notes

FlexiCap™ may be handled, stored and transported in the same manner as standard terminated capacitors. The requirements for mounting and soldering FlexiCap™ are the same as for standard SMD capacitors.

For customers currently using standard terminated capacitors there should be no requirement to change the assembly process when converting to FlexiCap™.

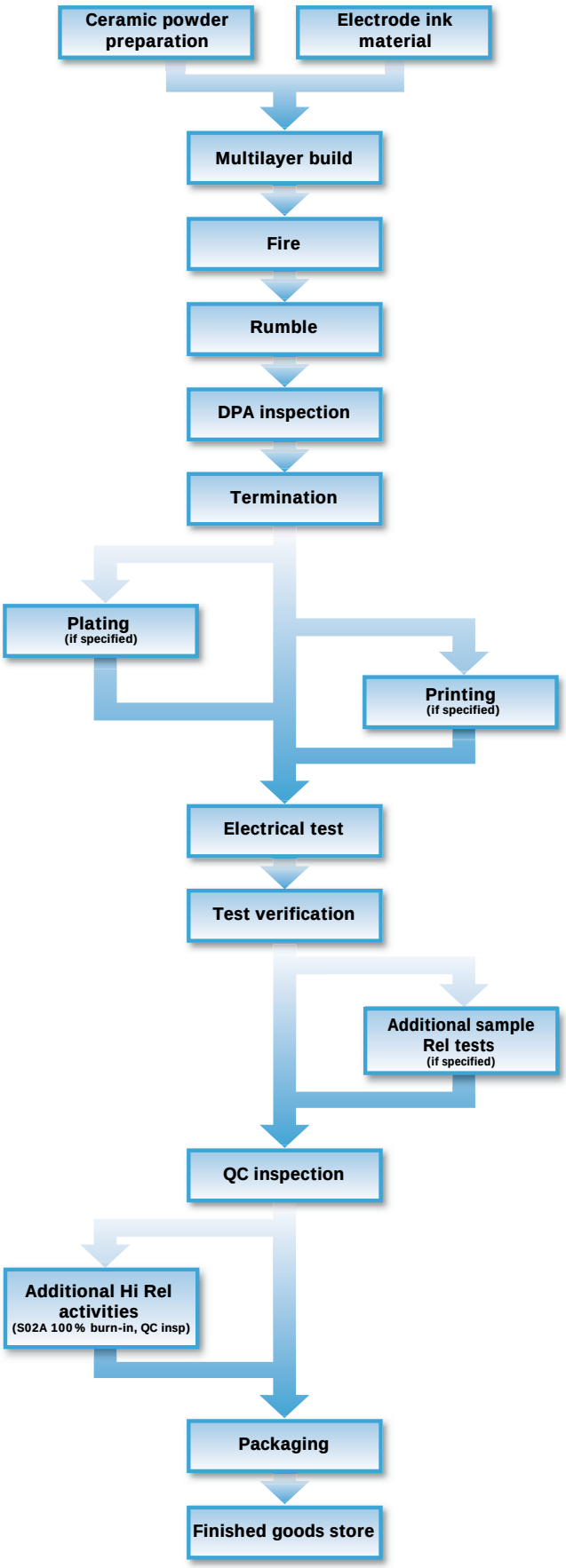
Based upon board bend tests in accordance with IEC 60384-1 the amount of board bending required to mechanically crack a FlexiCap™ terminated capacitor is significantly increased compared with standard terminated capacitors.

It must be stressed however, that capacitor users must not assume that the use of FlexiCap™ terminated capacitors will totally eliminate mechanical cracking. Good process controls are still required for this objective to be achieved.

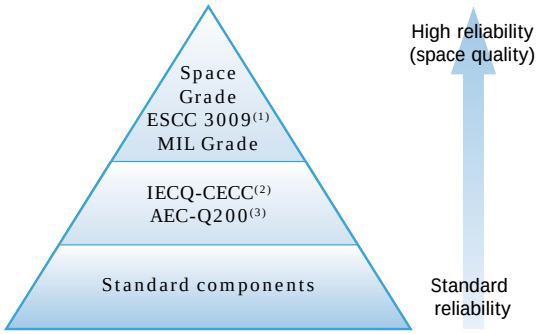
FlexiCap™

Manufacturing processes

Production process flowchart



Knowles reliability grades

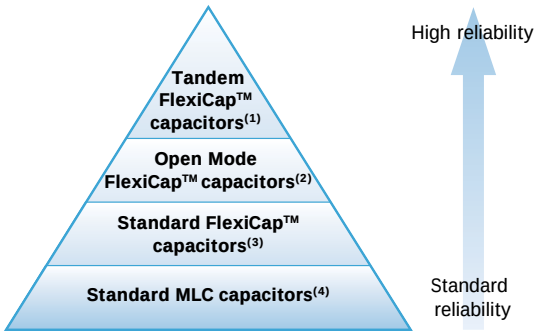


Notes:

1) Space grade tested in accordance with ESCC3009 (refer to Knowles Spec S02A 0100) or MIL Grade (in accordance with MIL-PRF-123, MIL-PRF-55681).
2) IECQ-CECC. The International Electrotechnical Commission (IEC) Quality Assessment System for Electronic Components. This is an internationally recognised product quality certification which provides customers with assurance that the product supplied meets high quality standards.

   View Knowles IECQ-CECC approvals at http://www.iecq.org or at www.knowlescapacitors.com
3) AEC-Q200. Automotive Electronics Council Stress Test Qualification For Passive Components. Refer to Knowles application note reference AN0009.

Knowles reliability surface mount product groups



Notes:

1) "Tandem" construction capacitors, ie internally having the equivalent of 2 series capacitors. If one of these should fail short-circuit, there is still capacitance end to end and the chip will still function as a capacitor, although capacitance maybe affected. Refer to application note AN0021. Also available qualified to AEC-Q200.
2) "Open Mode" capacitors with FlexiCap™ termination also reduce the possibility of a short circuit by utilising inset electrode margins. Refer to application note AN0022. Also available qualified to AEC-Q200.
3) Multilayer capacitors with Knowles FlexiCap™ termination. By using FlexiCap™ termination, there is a reduced possibility of the mechanical cracking occurring.
4) "Standard" capacitors includes MLCCs with tin finish over nickel but no FlexiCap™.

Testing

Tests conducted during batch manufacture

	Knowles reliability SM product group			
	Standard SM capacitors	IECQ-CECC / MIL grade	AEC-Q200	S (Space grade) High Rel S02A ESCC 3009 MIL-PRF-123
Solderability	●	●	●	●
Resistance to soldering heat	●	●	●	●
Plating thickness verification (if plated)	●	●	●	●
DPA (Destructive Physical Analysis)	●	●	●	●
Voltage proof test (DWV / Flash)	●	●	●	●
Insulation resistance	●	●	●	●
Capacitance test	●	●	●	●
Dissipation factor test	●	●	●	●
100% visual inspection	❍	❍	●	●
100% burn-in. (2xRV @125ºC for 168 hours)	❍	❍	❍	●
Load sample test @ 125ºC	❍	❍	●	LAT1 & LAT2 (1000 hours)
Humidity sample test. 85ºC/85%RH	❍	❍	●	240 hours
Hot IR sample test	❍	❍	❍	❍
Axial pull sample test (MIL-STD-123)	❍	❍	❍	❍
Breakdown voltage sample test	❍	❍	❍	❍
Deflection (bend) sample test	❍	❍	❍	❍
SAM (Scanning Acoustic Microscopy)	❍	❍	❍	❍
LAT1 (4 x adhesion, 8 x rapid temp change + LAT2 and LAT3)	-	-	-	❍
LAT2 (20 x 1000 hour life test + LAT3)	-	-	-	❍
LAT3 (6 x TC and 4 x solderability)	-	-	-	❍

● Test conducted as standard.
❍ Optional test. Please discuss with the Sales Office.

Periodic tests conducted for IECQ-CECC and AEC-Q200

Test ref	Test	Termination type	Additional requirements	Sample acceptance			Reference
				P	N	C	
P1	High temperature exposure (storage)	All types	Un-powered. 1,000 hours @ T=150ºC. Measurement at 24 ± 2 hours after test conclusion	12	77	0	MIL-STD-202 Method 108
P2	Temperature cycling	C0G/NP0: All types X7R: Y and H only	1,000 cycles -55ºC to +125ºC Measurement at 24 ± 2 hours after test conclusion	12	77	0	JESD22 Method JA-104
P3	Moisture resistance	All types	T = 24 hours/cycle. Note: Steps 7a and 7b not required. Un-powered. Measurement at 24 ± 2 hours after test conclusion	12	77	0	MIL-STD-202 Method 106
P4	Biased humidity	All types	1,000 hours 85ºC/85%RH. Rated voltage or 50V whichever is the least and 1.5V. Measurement at 24 ± 2 hours after test conclusion	12	77	0	MIL-STD-202 Method 103
P5	Operational life	All types	Condition D steady state TA=125ºC at full rated. Measurement at 24 ± 2 hours after test conclusion	12	77	0	MIL-STD-202 Method 108
P6	Resistance to solvents	All types	Note: Add aqueous wash chemical. Do not use banned solvents	12	5	0	MIL-STD-202 Method 215
P7	Mechanical shock	C0G/NP0: All types X7R: Y and H only	Figure 1 of Method 213. Condition F	12	30	0	MIL-STD-202 Method 213
P8	Vibration	C0G/NP0: All types X7R: Y and H only	5*g's* for 20 minutes, 12 cycles each of 3 orientations. Note: Use 8" x 5" PCB 0.031" thick 7 secure points on one long side and 2 secure points at corners of opposite sides. Parts mounted within 2" from any secure point. Test from 10-2,000Hz	12	30	0	MIL-STD-202 Method 204
P9	Resistance to soldering heat	All types	Condition B, no pre-heat of samples: Single wave solder - Procedure 2	3	12	0	MIL-STD-202 Method 210
P10	Thermal shock	C0G/NP0: All types X7R: Y and H only	-55ºC/+125ºC. Number of cycles 300. Maximum transfer time - 20 seconds, dwell time - 15 minutes. Air-Air	12	30	0	MIL-STD-202 Method 107
P11	Adhesion, rapid temp change and climatic sequence	X7R: A, F and J only	5N force applied for 10s, -55ºC/ +125ºC for 5 cycles, damp heat cycles	12	27	0	BS EN132100 Clause 4.8, 4.12 and 4.13
P12	Board flex	C0G/NP0: All types X7R: Y and H only	3mm deflection Class I 2mm deflection Class II	12	30	0	AEC-Q200-005
P13	Board flex	X7R: A, F and J only	1mm deflection.	12	12	0	BS EN132100 Clause 4.9
P14	Terminal strength	All types	Force of 1.8kg for 60 seconds	12	30	0	AEC-Q200-006
P15	Beam load test	All types	-	12	30	0	AEC-Q200-003
P16	Damp heat steady state	All types	56 days, 40ºC / 93% RH 15x no volts, 15x 5Vdc, 15x rated voltage or 50V whichever is the least.	12	45	0	BS EN132100 Clause 4.14

Test results are available on request.
P = Period in months.
N = Sample size.
C = Acceptance criteria.

High Reliability Testing

Our High Rel products are designed for optimum reliability and are burned in at elevated voltage and temperature levels. They are 100% electrically inspected to ascertain conformance to a strict performance criteria.

Applications for High Reliability products include medical implanted devices, aerospace, airborne, various military applications, and consumer uses requiring safety margins not attainable with conventional product.

We have the ability to test surface mount and leaded capacitors to High Reliability standards as detailed below, or to customer SCD.

Military performance specifications are designed and written for the voltage/capacitance ratings of the individual product slash numbers associated with the specification.

Some of the requirements of the military document may not apply to the High Reliability product. The following details the intent of the individual military specifications available for test and the deviations that may apply.

Product voltage ratings outside of the intended military specification will follow the voltage test potential outlined.

Contact the Sales Office with any requirements or deviations that are not covered here.

Environmental Testing

We also have the capability to perform all the Environmental Group B, Group C and Qualification testing to the referenced military specifications.

Testing abilities include the following:

- Nondestructive internal examination
- Destructive physical analysis
- Radiographic inspection
- Terminal strength
- Resistance to soldering heat
- Voltage-temperature limits
- Temperature coefficient
- Moisture resistance
- Humidity, steady state, low voltage
- Vibration
- Resistance to solvents
- Life
- Thermal shock and immersion
- Low temperature storage
- Barometric pressure
- Shock, specified pulse
- Mechanical shock
- Constant acceleration
- Wire bond evaluation
- Partial discharge (corona)
- 200°C Voltage Conditioning

Military Performance Specifications

MIL-PRF-55681 (GROUP A)

General purpose military high reliability specification for surface mount sizes 0805 through 2225 in 50V and 100V.

- VOLTAGE CONDITIONING
- 100 HRS, 2X VDCW, 125°C
- DWV, IR, 125°C IR, CAP, DF TEST
- VISUAL & MECH. INSPECTION (AQL SAMPLE PLAN)
- SOLDERABILITY, SAMPLE 13(0)
- 8% PDA MAXIMUM

MIL-PRF-123 (GROUP A)

The specification affords an increased reliability level over MIL-PRF-55681 for space, missile and other high reliability applications such as medical implantable or life support equipment. The specification covers surface mount sizes 0805 through 2225 in 50V rating and various radial / axial leaded products in 50V, 100V and 200V ratings.

- THERMAL SHOCK, 20 CYCLES
- VOLTAGE CONDITIONING 168/264 HRS, 2X VDCW, 125°C
- DWV, IR, 125°C IR, CAP, DF TEST
- VISUAL & MECH. INSPECTION SAMPLE 20(0)
- DPA(1)
- PDA, 3% (0.1%), 5% (0.2%) MAX(2)

MIL-PRF-39014 (GROUP A)

The specification covers general military purpose radial / axial leaded and encapsulated product in 50V, 100V, and 200V ratings.

- THERMAL SHOCK, 5 CYCLES
- VOLTAGE CONDITIONING 96 HRS, 2X VDCW, 125°C
- DWV, IR, 125°C IR, CAP, DF TEST
- VISUAL & MECH. INSPECTION (AQL SAMPLE PLAN)
- SOLDERABILITY, SAMPLE 13(0)
- 8% PDA MAXIMUM

MIL-PRF-49467 (GROUP A)

General purpose military high reliability specification for radial leaded epoxy coated. The specification covers sizes 1515 through 13060 with 600V, 1kV, 2kV, 3kV, 4kV and 5kV ratings.

- THERMAL SHOCK, 5 CYCLES
- VOLTAGE CONDITIONING 96 HRS, RATED VDCW, 125°C
- PARTIAL DISCHARGE (OPTION) (3)
- DWV, IR, 125°C IR, CAP, DF TEST
- VISUAL & MECH. INSPECTION SAMPLE 13(0)
- SOLDERABILITY, SAMPLE 5(0)
- 10% PDA MAXIMUM

MIL-PRF-49470 (DSCC 87106) (GROUP A)

General purpose military high reliability specification for stacked and leaded capacitors for switch mode power supplies. The specification covers sizes 2225 through 120200 in 50V, 100V, 200V and 500V ratings.

- THERMAL SHOCK, 5 CYCLES
- VOLTAGE CONDITIONING 96 HRS, 2X VDCW(4), 125°C
- DWV, IR, 125°C IR, CAP, DF TEST
- VISUAL & MECH. INSPECTION SAMPLE 13(0)
- SOLDERABILITY, SAMPLE 5(0)
- 10% PDA MAXIMUM

MIL-PRF-38534

Specification for Hybrid Microcircuits with a section for Element Evaluation on passive components.

There are two classification levels of reliability. Class H is for a standard military quality level. Class K is for the highest reliability level intended for space application.

Knowles will perform a 100-hour burn-in on all Class K products and assumes Class K Subgroup 3 samples will be unmounted and Subgroup 4 (wirebond) shall not apply unless otherwise stated.

TEST VOLTAGE (VDC)

This test potential shall be used on all High Reliability Testing unless otherwise specified.

WVDC	DWV	V/C*
<200	2.5X Rated	2.0X Rated
250	500V	400V
300	500V	400V
400	600V	500V
500	750V	600V
600	750V	600V
>700	1.2X Rated	1.0X Rated

*V/C Is Voltage Conditioning.

Notes:

1. MIL-PRF-123 DPA shall be per TABLE XIV AQL requirements unless otherwise specified.
2. MIL-PRF-123 allowable PDA shall be 3% overall and 0.1% in the last 48 hours for capacitance/voltage values listed in MIL-PRF-123, and be 5% overall and 0.2% in the last 48 hours for capacitance/voltage values beyond MIL-PRF-123.
3. MIL-PRF-49467 standard Group A is without Partial Discharge. Partial Discharge test is optional and must be specified.
4. MIL-PRF-49470 (DSCC 87106) 500V rated product has Voltage Conditioning at 1.2X VDCW.

Regulations and Compliance

Release documentation

	Knowles reliability SM product group			
	Standard SM capacitors	IECQ-CECC	AEC-Q200 MIL grade	S (Space grade) High Rel S02A
Certificate of conformance	●	-	●	●
IECQ-CECC Release certificate of conformity	-	●	-	-
Batch electrical test report	❍	❍	❍	Included in data pack
S (space grade) data documentation package	-	-	-	●

● Release documentation supplied as standard.
❍ Original documentation.

Periodic tests conducted and reliability data availability

Standard Surface Mount capacitors

Components are randomly selected on a sample basis and the following routine tests are conducted:

- Load Test. 1,000 hours @125ºC (150ºC for X8R). Applied voltage depends on components tested.
- Humidity Test. 168 hours @ 85ºC/85%RH.
- Board Deflection (bend test).

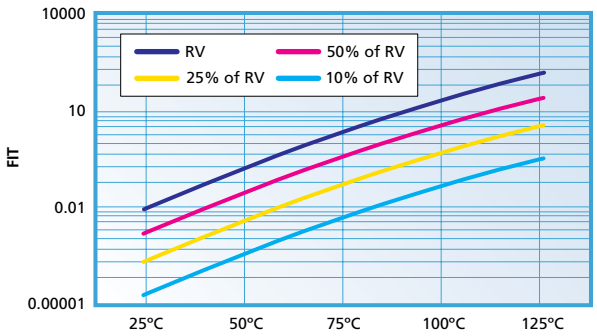
Test results are available on request.

Conversion factors

From	To	Operation
FITS	MTBF (hours)	$10^9 \div$ FITS
FITS	MTBF (years)	$10^9 \div$ (FITS x 8760)

FITS = Failures in 10^9 hours.
MTBF = Mean time between failures.

Example of FIT (Failure In Time) data available:



Component type: 0805 (C0G/NP0 and X7R).
Testing location: Knowles reliability test department.
Results based on: 16,622,000 component test hours.

REACH (Registration, Evaluation, Authorisation and restriction of Chemicals) statement

The main purpose of REACH is to improve the protection of human health and the environment from the risks arising from the use of chemicals.

Knowles maintains both ISO14001, Environmental Management System and OHSAS 18001 Health and Safety Management System approvals that require and ensure compliance with corresponding legislation such as REACH.

For further information, please contact the Knowles Capacitors Sales Office at www.knowlescapacitors.com

RoHS compliance

Knowles routinely monitors world wide material restrictions (e.g. EU/China and Korea RoHS mandates) and is actively involved in shaping future legislation.

All standard C0G/NP0, X7R, X5R and High Q Knowles MLCC products are compliant with the EU RoHS directive (see below for special exceptions) and those with plated terminations are suitable for soldering using common lead free solder alloys (refer to 'Soldering Information' for more details on soldering limitations). Compliance with the EU RoHS directive automatically signifies compliance with some other legislation (e.g. China and Korea RoHS). Please refer to the Knowles Capacitors Sales Office for details of compliance with other materials legislation.

Breakdown of material content, SGS analysis reports and tin whisker test results are available on request.

Most Knowles MLCC components are available with non RoHS compliant tin lead (SnPb) solderable termination finish for exempt applications and where pure tin is not acceptable. Other tin free termination finishes may also be available – please refer to the Knowles Capacitors Sales Office for further details.

Radial components have tin plated leads as standard but tin/lead is available as a special option. Please refer to the radial section of the catalogue for further details.

X8R ranges <250Vdc are not RoHS 2011/65/EU compliant. Check the website, www.knowlescapacitors.com for latest RoHS update.

Export controls and dual-use regulations

Certain Knowles catalogue components are defined as 'dual-use' items under international export controls - those that can be used for civil or military purposes which meet certain specified technical standards.

The defining criteria for a dual use component with respect to Knowles Capacitor products is one with a voltage rating of >750Vdc and a capacitance value of >250nF when measured at 750Vdc and a series inductance <10nH. Components defined as dual-use under the above criteria may require a licence for export across international borders. Please contact the Sales Office for further information on specific part numbers.

Explanation of Ageing of MLC

Ageing

Capacitor ageing is a term used to describe the negative, logarithmic capacitance change which takes place in ceramic capacitors with time. The crystalline structure for barium titanate based ceramics changes on passing through its Curie temperature (known as the Curie Point) at about 125°C. This domain structure relaxes with time and in doing so, the dielectric constant reduces logarithmically; this is known as the ageing mechanism of the dielectric constant. The more stable dielectrics have the lowest ageing rates.

The ageing process is reversible and repeatable. Whenever the capacitor is heated to a temperature above the Curie Point the ageing process starts again from zero.

The ageing constant, or ageing rate, is defined as the percentage loss of capacitance due to the ageing process of the dielectric which occurs during a decade of time (a tenfold increase in age) and is expressed as percent per logarithmic decade of hours. As the law of decrease of capacitance is logarithmic, this means that in a capacitor with an ageing rate of 1% per decade of time, the capacitance will decrease at a rate of:

a) 1% between 1 and 10 hours

b) An additional 1% between the following 10 and 100 hours

c) An additional 1% between the following 100 and 1000 hours

d) An additional 1% between the following 1000 and 10000 hours etc

e) The ageing rate continues in this manner throughout the capacitor's life.

Typical values of the ageing constant for our Multilayer Ceramic Capacitors are:

Dielectric class	Typical values
Ultra Stable C0G/NP0	Negligible capacitance loss through ageing
Stable X7R	<2% per decade of time

Capacitance measurements

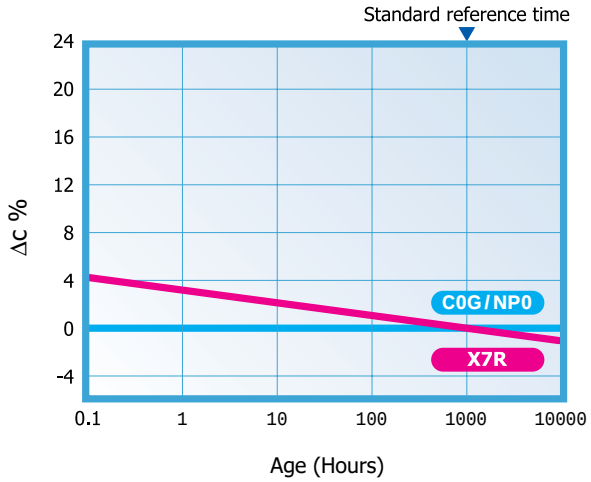
Because of ageing it is necessary to specify an age for reference measurements at which the capacitance shall be within the prescribed tolerance. This is fixed at 1000 hours, since for practical purposes there is not much further loss of capacitance after this time.

All capacitors shipped are within their specified tolerance at the standard reference age of 1000 hours after having cooled through their Curie temperature.

The ageing curve for any ceramic dielectric is a straight line when plotted on semi-log paper.

Capacitance vs time

(Ageing X7R @ <2% per decade)



Tight tolerance

One of the advantages of Knowles' unique 'wet process' of manufacture is the ability to offer capacitors with exceptionally tight capacitance tolerances.

The accuracy of the printing screens used in the fully automated, computer controlled manufacturing process allows for tolerance as close as +/-1% on C0G/NP0 parts greater than or equal to 10pF. For capacitance values below <4.7pF, tolerances can be as tight as +/-0.05pF.

Mounting, Soldering, Storage & Mechanical Precautions

Detailed application notes intended to guide and assist our customers in using multilayer ceramic capacitors in surface mount technology are available on the Knowles website www.knowlescapacitors.com

The information concentrates on the handling, mounting, connection, cleaning, test and re-work requirements particular to MLC's for SMD technology, to ensure a suitable match between component capability and user expectation. Some extracts are given below.

Mechanical considerations for mounted ceramic chip capacitors

Due to their brittle nature, ceramic chip capacitors are more prone to excesses of mechanical stress than other components used in surface mounting.

One of the most common causes of failure is directly attributable to bending the printed circuit board after solder attachment. The excessive or sudden movement of the flexible circuit board stresses the inflexible ceramic block causing a crack to appear at the weakest point, usually the ceramic/termination interface. The crack may initially be quite small and not penetrate into the inner electrodes; however, subsequent handling and rapid changes in temperature may cause the crack to enlarge.

This mode of failure is often invisible to normal inspection techniques as the resultant cracks usually lie under the capacitor terminations but if left, can lead to catastrophic failure. More importantly, mechanical cracks, unless they are severe may not be detected by normal electrical testing of the completed circuit, failure only occurring at some later stage after moisture ingression.

The degree of mechanical stress generated on the printed circuit board is dependent upon several factors including the board material and thickness; the amount of solder and land pattern. The amount of solder applied is important, as an excessive amount reduces the chip's resistance to cracking.

It is Knowles's experience that more than 90% are due to board depanelisation, a process where two or more circuit boards are separated after soldering is complete. Other manufacturing stages that should be reviewed include:

1) Attaching rigid components such as connectors, relays, display panels, heat sinks etc.
2) Fitting conventional leaded components. Special care must be exercised when rigid terminals, as found on large can electrolytic capacitors, are inserted.
3) Storage of boards in such a manner which allows warping.
4) Automatic test equipment, particularly the type employing "bed of nails" and support pillars.
5) Positioning the circuit board in its enclosure especially where this is a "snap-fit".

Knowles were the first MLCC manufacturer to launch a flexible termination to significantly reduce the instances of mechanical cracking. FlexiCap™ termination introduces a certain amount of give into the termination layer absorbing damaging stress. Unlike similar systems, FlexiCap™ does not tear under tension, but absorbs the stress, so maintaining the characteristics of the MLCC.

SM Pad Design

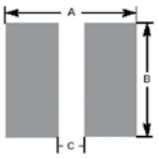
Knowles conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should also be considered.

3-Terminal components are not specifically covered by IPC-7351, but recommended pad dimensions are included in the Knowles catalogue / website for these components.

Alternative Printed Wire Board Land Patterns

Printed Wire Board land pattern design for chip components is critical to ensure a reliable solder fillet, and to reduce nuisance type manufacturing problems such as component swimming and tombstoning. The land pattern suggested can be used for reflow and wave solder operations as noted. Land patterns constructed with these dimensions will yield optimized solder fillet formation and thus reduce the possibility of early failure.[1]

A = (Max Length) + 0.030" (.762mm)*
B = (Max Width) + 0.010" (.254mm)**
C = (Min Length) – 2 (Nominal Band)***



* Add 0.030" for Wave Solder operations.
** Replace "Max Width" with "Max Thickness" for vertical mounting.
*** "C" to be no less than 0.02", change "A" to (Max Length) + 0.020".

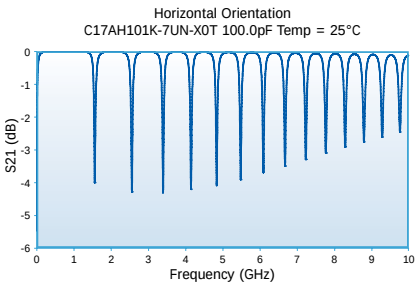
For C04 "C" to be no less than 0.01".

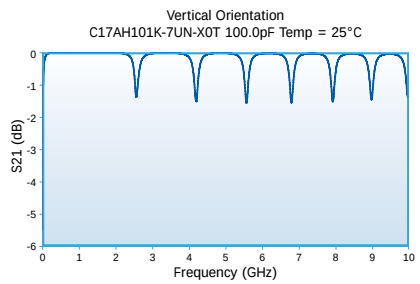
1. Frances Classon, James Root, Martin Marietta Orlando Aerospace, "Electronics Packaging and Interconnection Handbook".

MLC Orientation - Horizontal and Vertical Mounting

The orientation of the MLC relative to the ground plane affects the devices' impedance. When the internal electrodes are parallel to the ground plane (Horizontal mounting) the impedance of the MLC resembles a folded transmission line driven from one end.

The graphs below show the modeled insertion loss and parallel resonances of Knowles product C17AH101K-7UN-X0T with horizontal mounting (modeling can be done in CapCad). When the internal electrodes are perpendicular to the ground plane (Vertical mounting, bottom graph) the MLC impedance resembles a folded transmission line driven from the center reducing resonance effects.





Mounting, Soldering, Storage & Mechanical Precautions

Knowles MLCCs are compatible with all recognised soldering / mounting methods for chip capacitors.

Specific application notes on mounting and soldering Knowles components are included on the website for each brand.

- For DLI brand components please see DLI application note "Recommended Solder Attachment Techniques for MLC Chip and Pre-Tinned Capacitors" located at: **http://www.knowlescapacitors.com/dilabs/en/gn/resources/application-notes**
- For Syfer brand components, please see Syfer application note AN0028 "Soldering / Mounting Chip Capacitors, Radial Leaded Capacitors and EMI Filters" located at: **http://www.knowlescapacitors.com/syfer/en/gn/technical-info/application-notes**
- For Novacap brand products please refer to the appropriate application note located at: **http://www.knowlescapacitors.com/novacap/en/gn/technical-info/application-notes**

The volume of solder applied to the chip capacitor can influence the reliability of the device. Excessive solder can create thermal and tensile stresses on the component which can lead to fracturing of the chip or the solder joint itself. Insufficient or uneven solder application can result in weak bonds, rotation of the device off line or lifting of one terminal off the pad (tombstoning). The volume of solder is process and board pad size dependent.

Soldering methods commonly used in industry are Reflow Soldering, Wave Soldering and, to a lesser extent, Vapour Phase Soldering. All these methods involve thermal cycling of the components and therefore the rate of heating and cooling must be controlled to preclude thermal shocking of the devices.

Without mechanical restriction, thermally induced stresses are released once the capacitor attains a steady state condition. Capacitors bonded to substrates, however, will retain some stress, due primarily to the mismatch of expansion of the component to the substrate; the residual stress on the chip is also influenced by the ductility and hence the ability of the bonding medium to relieve the stress. Unfortunately, the thermal expansion of chip capacitors differ significantly from those of most substrate materials.

Large chips are more prone to thermal shock as their greater bulk will result in sharper thermal gradients within the device during thermal cycling. Large units experience excessive stress if processed through the fast cycles typical of solder wave or vapour phase operations.

Reflow soldering Surface Mount Chip Capacitors

Knowles recommend reflow soldering as the preferred method for mounting MLCCs. Knowles MLCCs can be reflow soldered using a reflow profile generally as defined in IPC / JEDEC J-STD-020. Sn plated termination chip capacitors are compatible with both conventional and lead free soldering, with peak temperatures of 260ºC to 270ºC acceptable.

The heating ramp rate should be such that components see a temperature rise of 1.5ºC to 4ºC per seconds to maintain temperature uniformity through the MLCC. The time for which the solder is molten should be maintained at a minimum, so as to prevent solder leaching. Extended times above 230ºC can cause problems with oxidation of Sn plating. Use of inert atmosphere can help if this problem is encountered. PdAg terminations can be particularly susceptible to leaching with lead free, tin rich solders and trials are recommended for this combination. Cooling to ambient temperature should be allowed to occur naturally, particularly if larger chip sizes are being soldered. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced cooling should be avoided as this can induce thermal breakage.

Wave soldering Surface Mount Chip Capacitors

Wave soldering is generally acceptable, but the thermal stresses caused by the wave have been shown to lead to potential problems with larger or thicker chips. Particular care should be taken when soldering SM chips larger than size 1210 and with a thickness greater than 1.0mm for this reason. 0402 size components are not suitable for wave soldering. 0402 size components can also be susceptible to termination leaching and reflow soldering is recommended for this size MLCC.

Wave soldering exposes the devices to a large solder volume, hence the pad size area must be restricted to accept an amount of solder which is not detrimental to the chip size utilized. Typically the pad width is 66% of the component width, and the length is .030" (.760 mm) longer than the termination band on the chip. An 0805 chip which is .050" wide and has a .020" termination band therefore requires a pad .033" wide by .050" in length. Opposing pads should be identical in size to preclude uneven solder fillets and mismatched surface tension forces which can misalign the device. It is preferred that the pad layout results in alignment of the long axis of the chips at right angles to the solder wave, to promote even wetting of all terminals. Orientation of components in line with the board travel direction may require dual waves with solder turbulence to preclude cold solder joints on the trailing terminals of the devices, as these are blocked from full exposure to the solder by the body of the capacitor.

The pre-heat ramp should be such that the components see a temperature rise of 1.5ºC to 4ºC per second as for reflow soldering. This is to maintain temperature uniformity through the MLCC and prevent the formation of thermal gradients within the ceramic. The preheat temperature should be within 120ºC maximum (100ºC preferred) of the maximum solder temperature to minimise thermal shock. Maximum permissible wave temperature is 270ºC for SM chips. Total immersion exposure time for Sn/Ni terminations is 30s at a wave temperature of 260ºC. Note that for multiple soldering operations, including the rework, the soldering time is cumulative.

The total immersion time in the solder should be kept to a minimum. It is strongly recommended that plated terminations are specified for wave soldering applications. PdAg termination is particularly susceptible to leaching when subjected to lead free wave soldering and is not generally recommended for this application.

Cooling to ambient temperature should be allowed to occur naturally, particularly if larger chip sizes are being soldered. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced cooling should be avoided as this can induce thermal breakage.

Vapour phase soldering Chip Capacitors

Vapour phase soldering can expose capacitors to similar thermal shock and stresses as wave soldering and the advice is generally the same. Particular care should be taken in soldering large capacitors to avoid thermal cracks being induced and natural cooling should be use to allow a gradual relaxation of stresses.

Hand soldering and rework of Chip Capacitors

Attachment using a soldering iron requires extra care and is accepted to have a risk of cracking of the chip. Precautions include preheating of the assembly to within 100°C of the solder flow temperature and the use of a fine tip iron which does not exceed 30 watts. In no circumstances should the tip of the iron be allowed to contact the chip directly.

Knowles recommend hot air/gas as the preferred method for applying heat for rework. Apply even heat surrounding the component to minimise internal thermal gradients.

Minimise the rework heat duration and allow components to cool naturally after soldering.

Mounting, Soldering, Storage & Mechanical Precautions

Wave soldering Radial Leaded Chip Capacitors

Radial leaded capacitors are suitable for wave soldering when mounted on the opposite side of the board to the wave. The body of radial components should not be exposed directly to the wave. Maximum permissible wave temperature is 260ºC for Radial Leaded capacitors.

Hand soldering Radial Leaded capacitors

Radial capacitors can be hand soldered into boards using soldering irons, provided care is taken not to touch the body of the capacitor with the iron tip. Soldering should be carried out from the opposite side of the board to the radial to minimise the risk of damage to the capacitor body. Where possible, a heat sink should be used between the solder joint and the body, especially if longer dwell times are required.

Solder leaching

Leaching is the term for the dissolution of silver into the solder causing a failure of the termination system which causes increased ESR, tan δ and open circuit faults, including ultimately the possibility of the chip becoming detached. Leaching occurs more readily with higher temperature solders and solders with a high tin content. Pb free solders can be very prone to leaching certain termination systems. To prevent leaching, exercise care when choosing solder alloys and minimize both maximum temperature and dwell time with the solder molten.

Plated terminations with nickel or copper anti leaching barrier layers are available in a range of top coat finishes to prevent leaching occurring. These finishes also include Syfer FlexiCap™ for improved stress resistance post soldering.

Bonding

Hybrid assembly using conductive epoxy or wire bonding requires the use of silver palladium or gold terminations. Nickel barrier termination is not practical in these applications, as intermetallics will form between the dissimilar metals. The ESR will increase over time and may eventually break contact when exposed to temperature cycling.

Cleaning

Chip capacitors can withstand common agents such as water, alcohol and degreaser solvents used for cleaning boards. Ascertain that no flux residues are left on the chip surfaces as these diminish electrical performance.

Handling

Ceramics are dense, hard, brittle and abrasive materials. They are liable to suffer mechanical damage, in the form of chips or cracks, if improperly handled.

Terminations may be abraded onto chip surfaces if loose chips are tumbled in bulk. Metallic tracks may be left on the chip surfaces which might pose a reliability hazard.

Components should never be handled with fingers; perspiration and skin oils can inhibit solderability and will aggravate cleaning.

Chip capacitors should never be handled with metallic instruments. Metal tweezers should never be used as these can chip the product and may leave abraded metal tracks on the product surface. Plastic or plastic coated metal types are readily available and recommended - these should be used with an absolute minimum of applied pressure.

Counting or visual inspection of chip capacitors is best performed on a clean glass or hard plastic surface.

If chips are dropped or subjected to rough handling, they should be visually inspected before use. Electrical inspection may also reveal gross damage via a change in capacitance, an increase in dissipation factor or a decrease either in insulation resistance or electrical strength.

Transportation

Where possible, any transportation should be carried out with the product in its unopened original packaging. If already opened, any environmental control agents supplied should be returned to packaging and the packaging re-sealed.

Avoid paper and card as a primary means of handling, packing, transportation and storage of loose components. Many grades have a sulphur content which will adversely affect termination solderability.

Loose chips should always be packed with sulphur-free wadding to prevent impact or abrasion damage during transportation.

Storage

Incorrect storage of components can lead to problems for the user. Rapid tarnishing of the terminations, with an associated degradation of solderability, will occur if the product comes into contact with industrial gases such as sulphur dioxide and chlorine. Storage in free air, particularly moist or polluted air, can result in termination oxidation.

Packaging should not be opened until the MLCs are required for use. If opened, the pack should be re-sealed as soon as is practicable. Alternatively, the contents could be kept in a sealed container with an environmental control agent.

Long term storage conditions, ideally, should be temperature controlled between -5 and +40°C and humidity controlled between 40 and 60% R.H.

Taped product should be stored out of direct sunlight, which might promote deterioration in tape or adhesive performance.

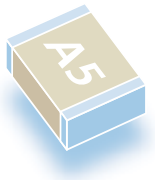
Product, stored under the conditions recommended above, in its "as received" packaging, has a minimum shelf life of 2 years.

Chip Marking System

If required, we can mark capacitors with the EIA 198 two digit code to show the capacitance value of the part. On chips larger than 3333, or for leaded encapsulated devices, ink marking is available. However, for chip sizes 0805 through to 3333 identification marking is accomplished by using either laser or ink jet printer. This system does not degrade the ceramic surface, or induce microcracks in the part.

Marking for other sizes may be available upon special request to determine if applicable; please contact the sales office.

Marking is an option on Novacap and Syfer branded products and needs to be specified when ordering.



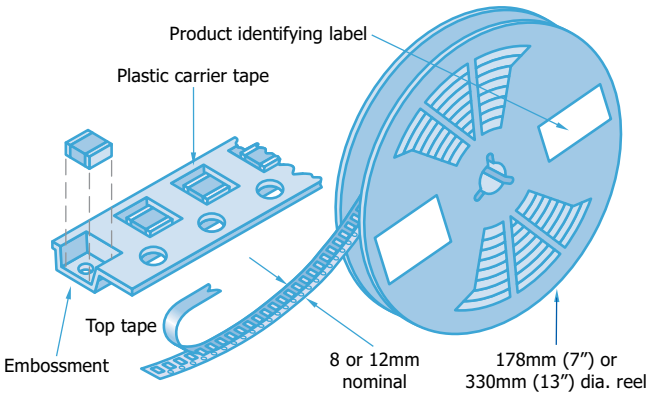
Two position alpha numeric marking is available on chip sizes 0805 through 3333.
The marking denotes retma value and significant figures of capacitance (see table) eg: A5 = 100,000pF.

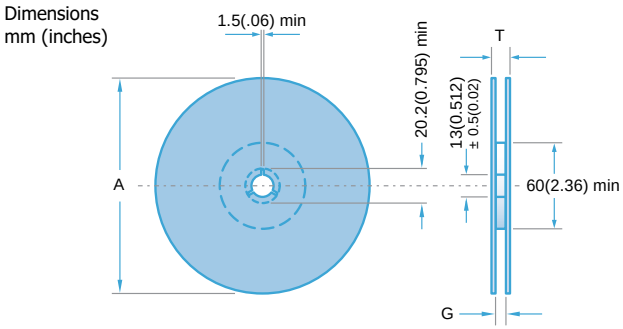
Three position alpha numeric marking is available on chip sizes 1206 and larger.
The making denotes Novacap as vendor (N), followed by the standard two digit alpha numeric identification.

Marking Code - value in picofarads for alpha-numeric code

Number		0	1	2	3	4	5	6	7	9
Letter	A	1.0	10	100	1,000	10,000	100,000	1,000,000	10,000,000	0.1
	B	1.1	11	110	1,100	11,000	110,000	1,100,000	11,000,000	0.11
	C	1.2	12	120	1,200	12,000	120,000	1,200,000	12,000,000	0.12
	D	1.3	13	130	1,300	13,000	130,000	1,300,000	13,000,000	0.13
	E	1.5	15	150	1,500	15,000	150,000	1,500,000	15,000,000	0.15
	F	1.6	16	160	1,600	16,000	160,000	1,600,000	16,000,000	0.16
	G	1.8	18	180	1,800	18,000	180,000	1,800,000	18,000,000	0.18
	H	2.0	20	200	2,000	20,000	200,000	2,000,000	20,000,000	0.2
	J	2.2	22	220	2,200	22,000	220,000	2,200,000	22,000,000	0.22
	K	2.4	24	240	2,400	24,000	240,000	2,400,000	24,000,000	0.24
	L	2.7	27	270	2,700	27,000	270,000	2,700,000	27,000,000	0.27
	M	3.0	30	300	3,000	30,000	300,000	3,000,000	30,000,000	0.3
	N	3.3	33	330	3,300	33,000	330,000	3,000,000	33,000,000	0.33
	P	3.6	36	360	3,600	36,000	360,000	3,600,000	36,000,000	0.36
	Q	3.9	39	390	3,900	39,000	390,000	3,900,000	39,000,000	0.39
	R	4.3	43	430	4,300	43,000	430,000	4,300,000	43,000,000	0.43
	S	4.7	47	470	4,700	47,000	470,000	4,700,000	47,000,000	0.47
	T	5.1	51	510	5,100	51,000	510,000	5,100,000	51,000,000	0.51
	U	5.6	56	560	5,600	56,000	560,000	5,600,000	56,000,000	0.56
	V	6.2	62	620	6,200	62,000	620,000	6,200,000	62,000,000	0.62
	W	6.8	68	680	6,800	68,000	680,000	6,800,000	68,000,000	0.68
	X	7.5	75	750	7,500	75,000	750,000	7,500,000	75,000,000	0.75
	Y	8.2	82	820	8,200	82,000	820,000	8,200,000	82,000,000	0.82
	Z	9.1	91	910	9,100	91,000	920,000	9,200,000	92,000,000	0.91
	a	2.5	25	250	2,500	25,000	250,000	2,500,000	25,000,000	0.25
	b	3.5	35	350	3,500	35,000	350,000	3,500,000	35,000,000	0.35
	d	4.0	40	400	4,000	40,000	400,000	4,000,000	40,000,000	0.4
	e	4.5	45	450	4,500	45,000	450,000	4,500,000	45,000,000	0.45
	f	5.0	50	500	5,000	50,000	500,000	5,000,000	50,000,000	0.5
	m	6.0	60	600	6,000	60,000	600,000	6,000,000	60,000,000	0.6
	n	7.0	70	700	7,000	70,000	700,000	7,000,000	70,000,000	0.7
	t	8.0	80	800	8,000	80,000	800,000	8,000,000	80,000,000	0.8
	y	9.0	90	900	9,000	90,000	900,000	9,000,000	90,000,000	0.9

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.





Symbol	Description	178mm reel	330mm reel
A	Diameter	178 (7)	330 (13)
G	Inside width	8.4 (0.33)	12.4 (0.49)
T	Outside width	14.4 (0.56) max	18.4 (0.72) max

Peel force

The peel force of the top sealing tape is between 0.2 and 1.0 Newton at 180°. The breaking force of the carrier and sealing tape in the direction of unreeling is greater than 10 Newtons.

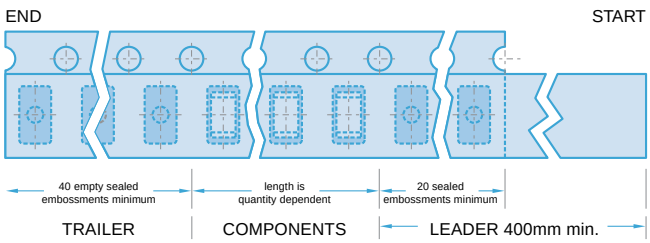
Identification

Each reel is labelled with the following information: manufacturer, chip size, capacitance, tolerance, rated voltage, dielectric type, batch number, date code and quantity of components.

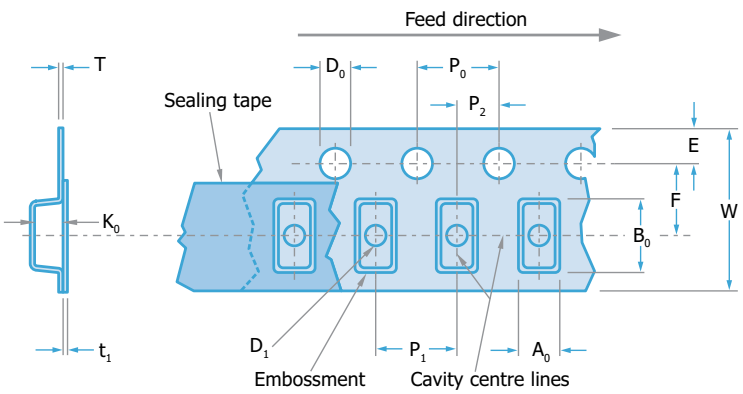
Missing components

Maximum number of missing components shall be 1 per reel or 0.025% whichever is greater. There shall not be consecutive components missing from any reel for any reason.

Leader and Trailer



Tape dimensions



		Dimensions mm (inches)	
Symbol	Description	8mm tape	12mm tape
A_0 B_0 K_0	Width of cavity Length of cavity Depth of cavity	Dependent on chip size to minimize rotation	
W	Width of tape	8.0 (0.315)	12.0 (0.472)
F	Distance between drive hole centres and cavity centres	3.5 (0.138)	5.5 (0.213)
E	Distance between drive hole centres and tape edge	1.75 (0.069)	
P_1	Distance between cavity centres	4.0 (0.156)	8.0 (0.315)
P_2	Axial distance between drive hole centres and cavity centres	2.0 (0.079)	
P_0	Axial distance between drive hole centres	4.0 (0.156)	
D_0	Drive hole diameter	1.5 (0.059)	
D_1	Diameter of cavity piercing	1.0 (0.039)	1.5 (0.059)
T	Carrier tape thickness	0.3 (0.012) ±0.1 (0.004)	0.4 (0.016) ±0.1 (0.004)
t_1	Top tape thickness	0.1 (0.004) max	

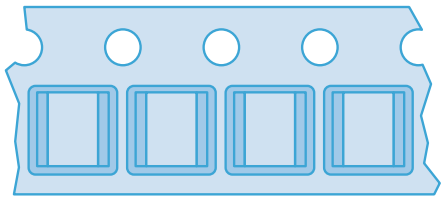
Ceramic Chip Capacitors - Packaging information

Component orientation

Tape and reeling is in accordance with IEC 60286 part 3, which defines the packaging specifications of lead less components on continuous tapes.

Notes: 1) IEC60286-3 states Ao ≤ Bo
(see tape dimensions on page 18).

2) Regarding the orientation of 1825 and 2225 components, the termination bands are right to left, NOT front to back. Please see diagram.

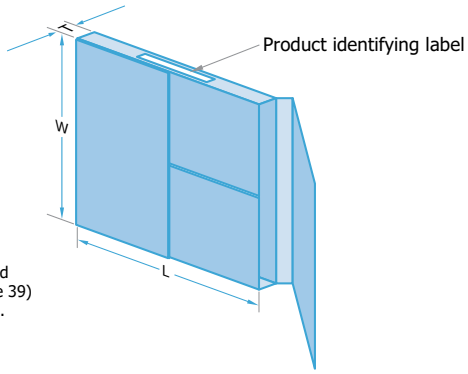


Orientation of 1825 & 2225 components

Outer Packaging

Outer carton dimensions mm (inches) max.

Reel Size	No. of reels	L	W	T
178 (7.0)	1	185 (7.28)	185 (7.28)	25 (0.98)
178 (7.0)	4	190 (7.48)	195 (7.76)	75 (2.95)
330 (13.0)	1	335 (13.19)	335 (13.19)	25 (0.98)



Note: Labelling of box and reel with bar codes (Code 39) available by arrangement.

Reel quantities - Novacap, Syfer and Voltronics products

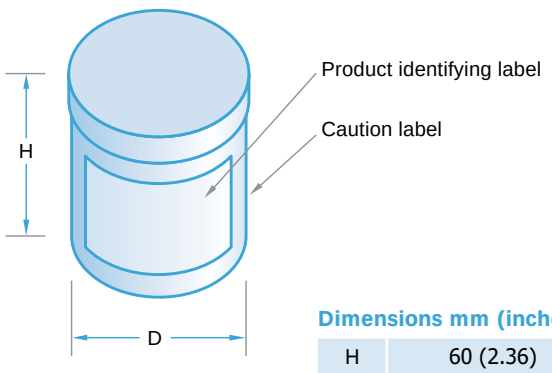
Chip size	0402	0505	0603	0805	1111	1206	1210	1410	1515	1808	1812	1825	2211	2215	2220	2221	2225	2520	3333	3530	3640	4540	5550	6560	7565
Max. chip thickness																									
mm	0.61	1.3	0.89	1.37	1.8	1.63	2.0	2.0	3.3	2.0	3.2	4.2	2.5	2.5	4.2	2.0	4.2	4.57	6.35	6.35	4.2	7.62	7.62	7.62	7.62
inches	0.02″	0.05″	0.03″	0.05″	0.07″	0.06″	0.08″	0.08″	0.13″	0.08″	0.13″	0.165″	0.1″	0.1″	0.165″	0.08″	0.165″	0.18″	0.25″	0.25″	0.165″	0.3″	0.3″	0.3″	0.3″
Reel quantities																									
178mm (7″)	10k	2500	4000	3000	1000	2500	2000	2000	500	1500	500	500	750	500	500	1000	500	1000	-	-	-	-		-	-
330mm (13″)	15k	10k	16k	12k	5000	10k	8000	8000	-	6000	2000	2000	4000	2000	2000	-	2000	1000	1000	500	500	500	500	500	200

Packaging configurations - DLI products

Chip size		7" Reel, 8mm Tape		7" Reel, 16mm Tape	13" Reel, 16mm Tape	2" x 2" Waffle Pack
Style	L x W	Horizontal Orientation	Vertical Orientation	Horizontal Orientation		
C04	0.040" x 0.020"	4000	-	-	-	-
C06	0.060" x 0.030"	4000	-	-	-	108
C07	0.110″ x 0.070″	2000	-	-	-	-
C08	0.080" x 0.050"	5000	3100	-	-	108
C11	0.055" x 0.055"	3500	3100	-	-	108
C17	0.110" x 0.110"	2350	750	-	-	49
C18	0.110" x 0.110"	2350	750	-	-	49
C22	0.220" x 0.245"	500	-	-	-	-
C40	0.380" x 0.380"	250	-	250	1300	-

Bulk packaging, tubs

Chips can be supplied in rigid re-sealable plastic tubs together with impact cushioning wadding. Tubs are labelled with the details: chip size, capacitance, tolerance, rated voltage, dielectric type, batch number, date code and quantity of components.

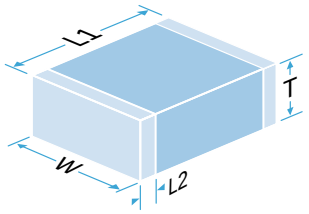


Dimensions mm (inches)

H	60 (2.36)
D	50 (1.97)

Chip dimensions

1. For FlexiCap™ terminations, length increase by maximum 0.004" (0.1mm).
2. For special ranges, inc. High Q and Ultra-low ESR, dimensions may vary. See individual catalogue page.
3. High Q and Ultra-low ESR ranges dimensions may vary for optimum performance.
4. Non-standard thicknesses are available – consult local Knowles Capacitors Sales Office.



Size	Length (L1)	Width (W)	Max. Thickness (T)	Termination Band (L2)	
	mm ~ inches	mm ~ inches	mm ~ inches	min (mm ~ inches)	max (mm ~ inches)
0402	1.0 ± 0.10 ~ 0.04 ± 0.004	0.50 ± 0.10 ~ 0.02 ± 0.004	0.60 ~ 0.024	0.10 ~ 0.004	0.40 ~ 0.016
C04	1.057 ± 0.188 ~ 0.042 ± 0.008	0.515 ± 0.153 ~ 0.02 ± 0.006	0.64 ~ 0.025	0.097 ~ 0.004	0.427 ~ 0.017
0504	1.27 ± 0.152 ~ 0.050 ± 0.006	1.02 ± 0.152 ~ 0.04 ± 0.006	1.12 ~ 0.044	0.20 ~ 0.008	0.50 ~ 0.02
0505	1.4 +0.35 -0.25 ~ 0.055 +0.014 -0.01	1.4 ± 0.25 ~ 0.055 ± 0.01	1.27 ~ 0.05	0.13 ~ 0.005	0.5 ~ 0.02
RF0505	1.4 ± 0.13 ~ 0.055 ± 0.005	1.4 ± 0.381 ~ 0.055 ± 0.015	1.45 ~ 0.057	0.20 ~ 0.008	0.50 ~ 0.02
C11	1.477 ± 0.391 ~ 0.059 ± 0.016	1.416 ± 0.451 ~ 0.056 ± 0.018	1.334 ~ 0.053	0.193 ~ 0.008	0.733 ~ 0.029
0603	1.6 ± 0.15 ~ 0.063 ± 0.006	0.8 ± 0.15 ~ 0.032 ± 0.006	0.90 ~ 0.036	0.20 ~ 0.004	0.40 ~ 0.016
C06	1.532 ± 0.229 ~ 0.06 ± 0.009	0.77 ± 0.191 ~ 0.031 ± 0.008	0.8 ~ 0.032	0.169 ~ 0.007	0.680 ~ 0.027
C07	1.797 ± 0.470 ~ 0.071 ± 0.019	2.813 ± 0.521 ~ 0.111 ± 0.021	2.667 ~ 0.105	0.193 ~ 0.008	1.20 ~ 0.047
0805	2.0 ± 0.20 ~ 0.079 ± 0.008	1.25 ± 0.20 ~ 0.049 ± 0.008	1.37 ~ 0.054	0.25 ~ 0.010	0.75 ~ 0.030
C08	2.048 ± 0.407 ~ 0.081 ± 0.016	1.28 ± 0.267 ~ 0.051 ± 0.011	1.360 ~ 0.054	0.362 ~ 0.014	1.04 ~ 0.041
0907	2.3 ± 0.30 ~ 0.090 ± 0.012	1.8 ± 0.30 ~ 0.070 ± 0.012	1.52 ~ 0.06	0.25 ~ 0.010	0.75 ~ 0.030
1005	2.54 ± 0.203 ~ 0.100 ± 0.008	1.27 ± 0.203 ~ 0.050 ± 0.008	1.37 ~ 0.054	0.25 ~ 0.010	0.75 ~ 0.030
1111	2.79 +0.51 -0.25 ~ 0.11 +0.02 -0.01	2.79 ± 0.38 ~ 0.113 ± 0.015	1.78 ~ 0.07	0.13 ~ 0.005	0.63 ~ 0.025
RF1111	2.79 ± 0.39 ~ 0.110 ± 0.005	2.79 ± 0.381 ~ 0.110 ± 0.015	2.59 ~ 0.102	0.25 ~ 0.010	0.75 ~ 0.030
C17	2.94 ± 0.527 ~ 0.116 ± 0.021	2.813 ± 0.521 ~ 0.111 ± 0.021	2.667 ~ 0.105	0.193 ~ 0.008	1.2 ~ 0.047
C18	3.14 ± 0.727 ~ 0.124 ± 0.029	2.946 ± 0.654 ~ 0.116 ± 0.026	2.667 ~ 0.105	0.193 ~ 0.008	1.2 ~ 0.047
1206	3.2 ± 0.20 ~ 0.126 ± 0.008	1.6 ± 0.20 ~ 0.063 ± 0.008	1.70 ~ 0.068	0.25 ~ 0.010	0.75 ~ 0.030
1210	3.2 ± 0.20 ~ 0.126 ± 0.008	2.5 ± 0.20 ~ 0.098 ± 0.008	2.0 ~ 0.08	0.25 ~ 0.010	0.75 ~ 0.030
1515	3.81 ± 0.381 ~ 0.150 ± 0.015	3.81 ± 0.381 ~ 0.150 ± 0.015	3.3 ~ 0.13	0.381 ~ 0.015	1.143 ~ 0.045
1808	4.5 ± 0.35 ~ 0.180 ± 0.014	2.0 ± 0.30 ~ 0.08 ± 0.012	2.0 ~ 0.08	0.25 ~ 0.01	1.0 ~ 0.04
1812	4.5 ± 0.30 ~ 0.180 ± 0.012	3.2 ± 0.20 ~ 0.126 ± 0.008	3.2 ~ 0.125	0.25 ~ 0.010	1.143 ~ 0.045
1825	4.5 ± 0.30 ~ 0.180 ± 0.012	6.40 ± 0.40 ~ 0.252 ± 0.016	4.2 ~ 0.16	0.25 ~ 0.010	1.0 ~ 0.04
2020	5.0 ± 0.40 ~ 0.197 ± 0.016	5.0 ± 0.40 ~ 0.197 ± 0.016	4.5 ~ 0.18	0.25 ~ 0.01	1.0 ~ 0.04
2220	5.7 ± 0.40 ~ 0.225 ± 0.016	5.0 ± 0.40 ~ 0.197 ± 0.016	4.2 ~ 0.165	0.25 ~ 0.01	1.0 ~ 0.04
2211	5.7 ± 0.40 ~ 0.225 ± 0.016	2.79 ± 0.30 ~ 0.11 ± 0.012	2.5 ~ 0.1	0.25 ~ 0.01	0.8 ~ 0.03
2215	5.7 ± 0.40 ~ 0.225 ± 0.016	3.81 ± 0.35 ~ 0.35 ± 0.02	2.5 ~ 0.1	0.25 ~ 0.01	0.8 ~ 0.03
2221	5.59 ± 0.381 ~ 0.220 ± 0.015	5.33 ± 0.381 ~ 0.210 ± 0.015	2.03 ~ 0.08	0.381 ~ 0.015	1.143 ~ 0.045
2225	5.7 ± 0.40 ~ 0.225 ± 0.016	6.30 ± 0.40 ~ 0.252 ± 0.016	4.2 ~ 0.165	0.381 ~ 0.01	1.143 ~ 0.045
C22	5.734 ± 0.667 ~ 0.226 ± 0.026	6.37 ± 0.699 ~ 0.251 ± 0.028	3.467 ~ 0.137	N/A	N/A
2520	6.35 ± 0.40 ~ 0.250 ± 0.016	5.08 ± 0.40 ~ 0.200 ± 0.016	4.57 ~ 0.18	0.381 ~ 0.015	1.143 ~ 0.045
RF2525	5.84 ± 0.21 ~ 0.230 ± 0.008	6.35 ± 0.381 ~ 0.250 ± 0.015	4.19 ~ 0.165	0.381 ~ 0.015	1.143 ~ 0.045
3333	8.38 ± 0.432 ~ 0.330 ± 0.017	8.38 ± 0.432 ~ 0.330 ± 0.017	6.35 ~ 0.25	0.381 ~ 0.015	1.143 ~ 0.045
3530	8.89 ± 0.457 ~ 0.350 ± 0.018	7.62 ± 0.381 ~ 0.300 ± 0.015	6.35 ~ 0.25	0.381 ~ 0.015	1.143 ~ 0.045
3640	9.2 ± 0.50 ~ 0.36 ± 0.02	10.16 ± 0.50 ~ 0.40 ± 0.02	4.5 ~ 0.18	0.50 ~ 0.02	1.50 ~ 0.06
C40	9.732 ± 0.804 ~ 0.384 ± 0.032	8.665 ± 1.737 ~ 0.381 ± 0.029	3.467 ~ 0.137	N/A	N/A
4040	10.2 ± 0.508 ~ 0.400 ± 0.020	10.2 ± 0.508 ~ 0.400 ± 0.020	7.62 ~ 0.30	0.50 ~ 0.02	1.50 ~ 0.06
4540	11.4 ± 0.584 ~ 0.450 ± 0.023	10.2 ± 0.508 ~ 0.400 ± 0.020	7.62 ~ 0.30	0.50 ~ 0.02	1.50 ~ 0.06
5440	13.7 ± 0.686 ~ 0.540 ± 0.027	10.2 ± 0.508 ~ 0.400 ± 0.020	7.62 ~ 0.30	0.50 ~ 0.02	1.50 ~ 0.06
5550	14.0 ± 0.711 ~ 0.550 ± 0.028	12.7 ± 0.635 ~ 0.500 ± 0.025	7.62 ~ 0.30	0.50 ~ 0.02	1.50 ~ 0.06
6560	16.5 ± 0.838 ~ 0.650 ± 0.033	15.2 ± 0.762 ~ 0.600 ± 0.030	7.62 ~ 0.30	0.50 ~ 0.02	1.50 ~ 0.06
7565	19.1 ± 0.965 ~ 0.750 ± 0.038	16.5 ± 0.838 ~ 0.650 ± 0.033	7.62 ~ 0.30	0.50 ~ 0.02	1.50 ~ 0.06
8060	20.3 ± 0.5 ~ 0.80 ± 0.02	15.24 ± 0.50 ~ 0.60 ± 0.02	4.2 ~ 0.165	0.50 ~ 0.02	1.50 ~ 0.06